IN THE TITLE

Please delete the present Title of the Invention and insert in place thereof the following Title, --METHOD FOR A JUNCTION FIELD EFFECT TRANSISTOR WITH REDUCED GATE CAPACITANCE--.

LISTING OF THE CLAIMS

A detailed listing of claims is presented below. Please amend currently amended claims as indicated below including substituting clean versions for pending claims with the same number. In addition, clean text versions of pending claims not being currently amended that are under examination are also presented. It is understood that any claim presented in a clean version below has not been changed relative to the immediate prior version.

1. Cancelled in Transmittal.

2. Cancelled in Transmittal.

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14. Previously canceled.

15. Cancelled in Transmittal.

16. Cancelled in Transmittal.

17. (Original) A method of fabricating a junction field effect transistor (JFET) comprising:

a) on an n^{++} substrate, forming an n-type epitaxial layer comprising a dopant concentration less than said n^{++} substrate;

b) forming a n^{+} source region disposed on top of a surface of said n-type epitaxial layer, said n^{+} source region having a dopant

concentration in between said n^{++} substrate and said n-type epitaxial layer;

c) forming a plurality of well regions in said n-type epitaxial layer surrounding said n^{+} source region;

d) forming a plurality of p-type gate regions surrounding bottoms of said plurality of well regions in said n-type epitaxial layer; and

e) forming an altered n-type epitaxial region below said plurality of well regions for extending depletion regions surrounding said plurality of p-type gate regions into said n-type epitaxial layer without compromising an active region of said JFET.

18. (Original) The method of fabricating a JFET as described in Claim 17, further comprising:

before e), forming an oxide spacer on walls of at least one of said plurality of well regions that extend down from said surface into said n-type epitaxial region for directing dopants into said altered n-type epitaxial region in step e).

19. (Currently Amended) The method of fabricating a JFET as described in Claim 18, further comprising:

filling <u>at least one of</u> said well region<u>s</u> with oxide.

20. (Currently Amended) The method of fabricating a JFET as described in Claim 17, wherein e) comprises:

implanting a lightly doped n^- layer directly below said plurality of well regions, said lightly doped n^- layer comprising a second dopant concentration less than that of said n-type epitaxial layer.

21. (Currently Amended) The method of fabricating a JFET as described in Claim 17, wherein e) comprises:

implanting a lightly doped p^- layer directly below said plurality of well regions, said lightly doped p^- layer comprising a second dopant concentration less than that of said p-type gate region.

22. (Original) A method of fabricating a junction field effect transistor (JFET) comprising:

a) on an p^{++} substrate, forming an p-type epitaxial layer comprising a dopant concentration less than said p^{++} substrate;

b) forming a p^+ source region disposed on top of a surface of said p-type epitaxial layer, said p^+ source region comprising a dopant concentration in between said p^{++} substrate and said p-type epitaxial layer;

c) forming a plurality of well regions in said p-type epitaxial layer surrounding said p^+ source region;

d) forming a plurality of n-type gate regions surrounding bottoms of said plurality of well regions in said p-type epitaxial layer; and

e) forming an altered p-type epitaxial region below said plurality of well regions for extending depletion regions

surrounding said plurality of n-type gate regions into said p-type epitaxial layer without compromising an active region of said JFET.

23. (Original) The method of fabricating a JFET as described in Claim 22, further comprising:

filling said well region with oxide.

24. (Original) The method of fabricating a JFET as described in Claim 22, further comprising:

before e), forming an oxide spacer on walls of at least one of said plurality of well regions, said walls extending down from said surface into said p-type epitaxial region for directing dopants into said altered p-type epitaxial region in step e).

25. (Original) The method of fabricating a JFET as described in Claim 22, wherein e) comprises:

implanting a lightly doped p^- layer directly below said well region, said lightly doped p^- layer comprising a second dopant concentration less than that of said p-type epitaxial layer.

26. (Original) The method of fabricating a JFET as described in Claim 22, wherein e) comprises:

implanting a lightly doped n^- layer directly below said well region, said lightly doped n^- layer comprising a second dopant concentration less than that of said n-type gate region.

27. (New) A method for forming a junction field effect transistor (JFET) comprising:

forming a drain region comprising a heavily doped n^{++} substrate;

forming an epitaxial n layer comprising a dopant concentration less than that of said n^{++} substrate, said epitaxial n layer formed on top of said n^{++} substrate;

forming a control structure comprising a p-type gate region implanted into said epitaxial n layer;

forming a source region sharing a p-n junction with said p-type gate region; and

forming an altered epitaxial region below said p-type gate region for enlarging a depletion region surrounding said p-type gate region, wherein said altered epitaxial region comprises a lightly doped p^- layer, wherein said lightly doped p^- layer comprises a second dopant concentration less than that of said p-type gate region.

28. (New) The method of Claim 27, further comprising:

implanting said lightly doped p^- layer at a higher energy than that associated with said p-type gate region.

29. (New) The method of Claim 27, further comprising:

forming a well region below a surface of said epitaxial n layer, said oxide well region above said p-type gate region; and

forming an oxide spacer on walls of said well region extending from a surface of said epitaxial n layer down into said

epitaxial n layer, said oxide spacer for directing implantation of dopants into said altered epitaxial region.

30. (New) The method of Claim 29, further comprising:

filling said well region with oxide.

31. (New) The method of Claim 27, further comprising:

reducing a junction capacitance between said p-type gate region and said drain region by further extending said depletion region into said epitaxial n layer, without compromising an active region of said JFET.

32. (New) A method for forming a junction field effect transistor (JFET) comprising:

forming a heavily doped p^{++} substrate forming a drain region;

forming an epitaxial p layer comprising a dopant concentration less than that of said p^{++} substrate, said epitaxial p layer formed on top of said p^{++} substrate;

forming a control structure comprising a n-type gate region implanted into said epitaxial p layer;

forming a source region sharing a p-n junction with said n-type gate region; and

forming an altered epitaxial region below said n-type gate region for widening a enlarging region surrounding said n-type gate region, wherein said altered epitaxial region comprises a lightly doped n^- layer, wherein said lightly doped n^- layer

comprises a second dopant concentration less than that of said n-type gate region.

33. (New) The method of Claim 32, further comprising:

implanting said lightly doped n^- layer at a higher energy than that associated with said n-type gate region.

34. (New) The method of Claim 32, further comprising:

forming a well region below a surface of said epitaxial p layer, said oxide well region above said n-type gate region; and

forming an oxide spacer on an approximately vertical surface between said well region and said epitaxial p layer, said oxide spacer for directing implantation of dopants into said altered epitaxial region.

35. (New) The method of Claim 34, further comprising:

filling said well region with oxide.

36. (New) The method of Claim 32, further comprising:

reducing a junction capacitance between said n-type gate region and said drain region by further extending said depletion region into said epitaxial p layer, without compromising an active region of said JFET.